Silicon N-Channel Power MOSFET

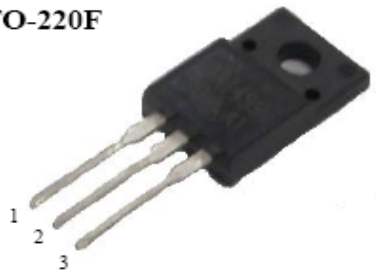
CS10N65FA9HD

V_{DSS}	650	V
I_D	10	A
P_D (T_C=25℃)	50	W
$R_{DS(ON)Typ}$	0.75	Ω

General Description:

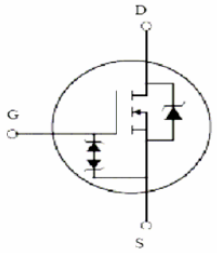
CS10N65FA9HD, the silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-220F, which accords with the RoHS standard.

TO-220F



1. Gate 2. Drain 3. Source

Inner Equivalent Principium Chart



Features:

- **Fast Switching**
- **ESD Improved Capability**
- **Low Gate Charge (Typical Data:38nC)**
- **Low Reverse transfer capacitances(Typical:15pF)**
- **100% Single Pulse avalanche energy Test**

Applications:

Power switch circuit of adaptor and charger.

Absolute（Tc= 25℃ unless otherwise specified）:

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	650	V
I_D	Continuous Drain Current	10	A
	Continuous Drain Current T_C = 100 °C	6.4	A
I_{DM} [a1]	Pulsed Drain Current	40	A
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS} [a2]	Single Pulse Avalanche Energy	700	mJ
E_{AR} [a1]	Avalanche Energy ,Repetitive	70	mJ
I_{AR} [a1]	Avalanche Current	3.7	A
dv/dt [a3]	Peak Diode Recovery dv/dt	5.0	V/ns
P_D	Power Dissipation	50	W
	Derating Factor above 25°C	0.4	W/℃
$V_{ESD(G-S)}$	Gate source ESD (HBM-C= 100pF, R=1.5kΩ)	4000	V
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, –55 to 150	℃
T_L	MaximumTemperature for Soldering	300	℃

Electrical Characteristics（Tc= 25℃ unless otherwise specified）：

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	650	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Bvdss Temperature Coefficient	ID=250uA,Reference25℃	--	0.74	--	V/℃
I_{DSS}	Drain to Source Leakage Current	V_{DS} = 650V, V_{GS}= 0V, T_a = 25℃	--	--	25	μA
		V_{DS} =520V, V_{GS}= 0V, T_a = 125℃	--	--	250	
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS} =+30V	--	--	10	μA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS} =-30V	--	--	-10	μA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}=10V,I_D=5A	--	0.75	0.85	Ω
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	2.0		4.0	V
Pulse width tp≤380μs, δ ≤2%						

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g_{fs}	Forward Transconductance	V_{DS}=15V, I_D =5.0A	--	11	--	S
C_{iss}	Input Capacitance	V_{GS} = 0V V_{DS} = 25V f = 1.0MHz	--	1758	--	pF
C_{oss}	Output Capacitance		--	153	--	
C_{rss}	Reverse Transfer Capacitance		--	15	--	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	I_D =10.0A V_{DD} = 325V V_{GS} = 10V R_G = 4.7Ω	--	20	--	ns
tr	Rise Time		--	20	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	55	--	
t_f	Fall Time		--	30	--	
Q_g	Total Gate Charge	I_D =10.0A V_{DD} =325V V_{GS} = 10V	--	38		nC
Q_{gs}	Gate to Source Charge		--	8.7	--	
Q_{gd}	Gate to Drain (“Miller”)Charge		--	15	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)		--	--	10	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	40	A
V_{SD}	Diode Forward Voltage	I_S=10.0A,V_{GS}=0V	--	--	1.5	V
trr	Reverse Recovery Time	I_S=10.0A,T_j = 25° C dI$_F$/dt=100A/us, V_{GS}=0V	--	434	--	ns
Qrr	Reverse Recovery Charge		--	2.6	--	nC
I_{RRM}	Reverse Recovery Current		--	12.2	--	A
Pulse width tp≤380μs, δ ≤2%						

Symbol	Parameter	Typ.	Units
$R_{\theta JC}$	Junction-to-Case	2.5	℃/W
$R_{\theta JA}$	Junction-to-Ambient	100	℃/W

Gate-source Zener diode						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{GSO}	Gate-source breakdown voltage	I_{GS}= ±1mA(Open Drain)	20			V
The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.						

[a1]: Repetitive rating; pulse width limited by maximum junction temperature
[a2]: L=10.0mH, I_D=12.6A, Start T_J=25℃
[a3]: I_{SD} =10A,di/dt ≤100A/us,V_{DD}≤$BV_{DS,}$ Start T_J=25℃

Characteristics Curve:

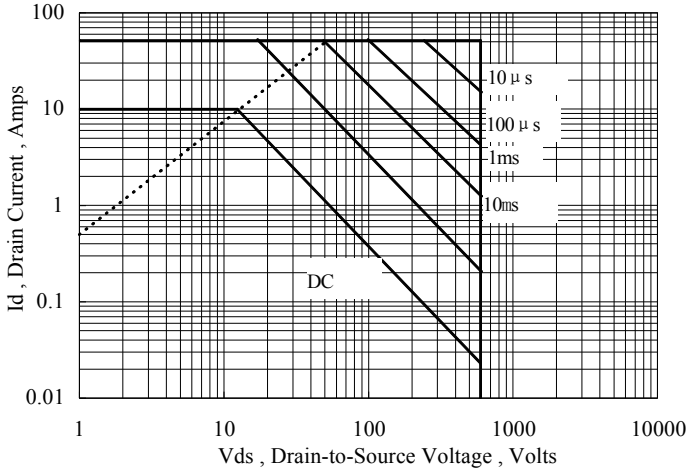


Figure 1 Maximun Forward Bias Safe Operating Area

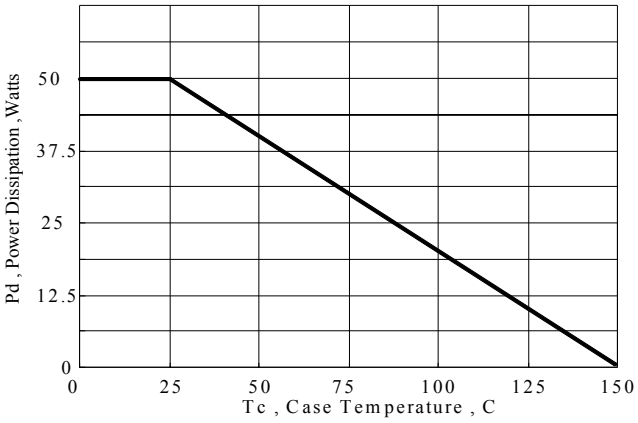


Figure 2 Maximun Power Dissipation vs Case Temperature

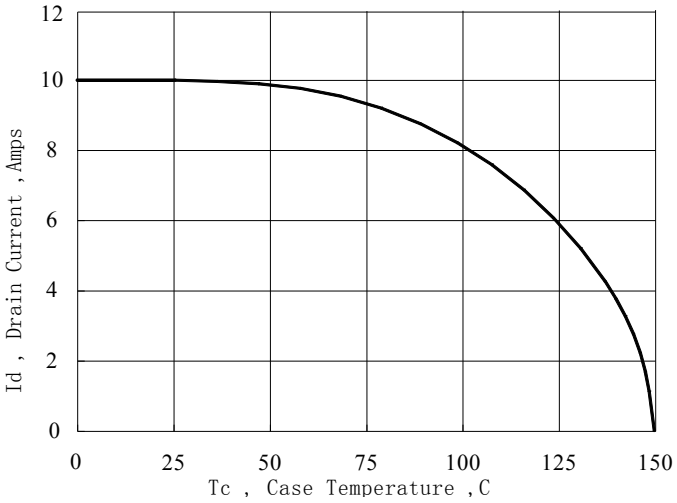


Figure 3 Maximum Continuous Drain Current vs Case Temperature

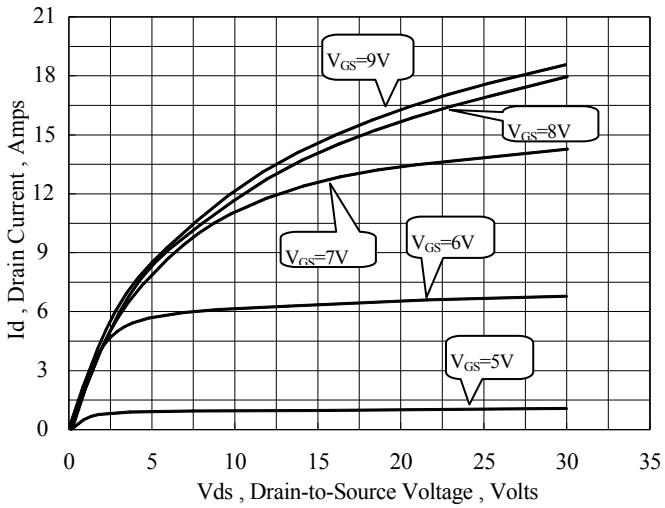


Figure 4 Typical Output Characteristics

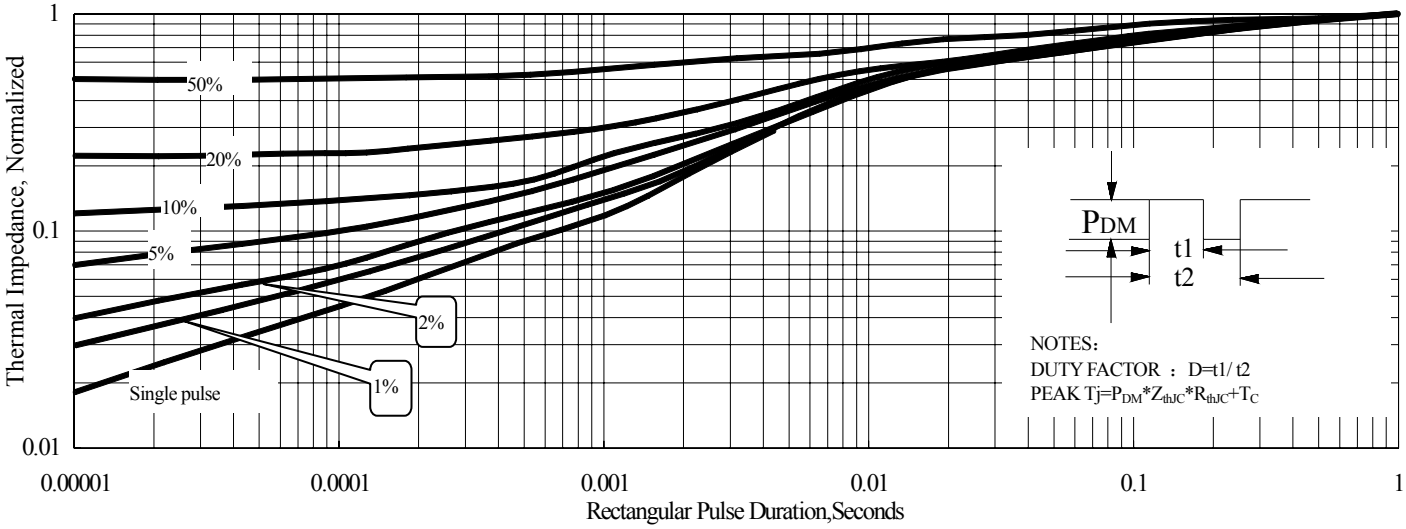


Figure 5 Maximum Effective Thermal Impendance , Junction to Case

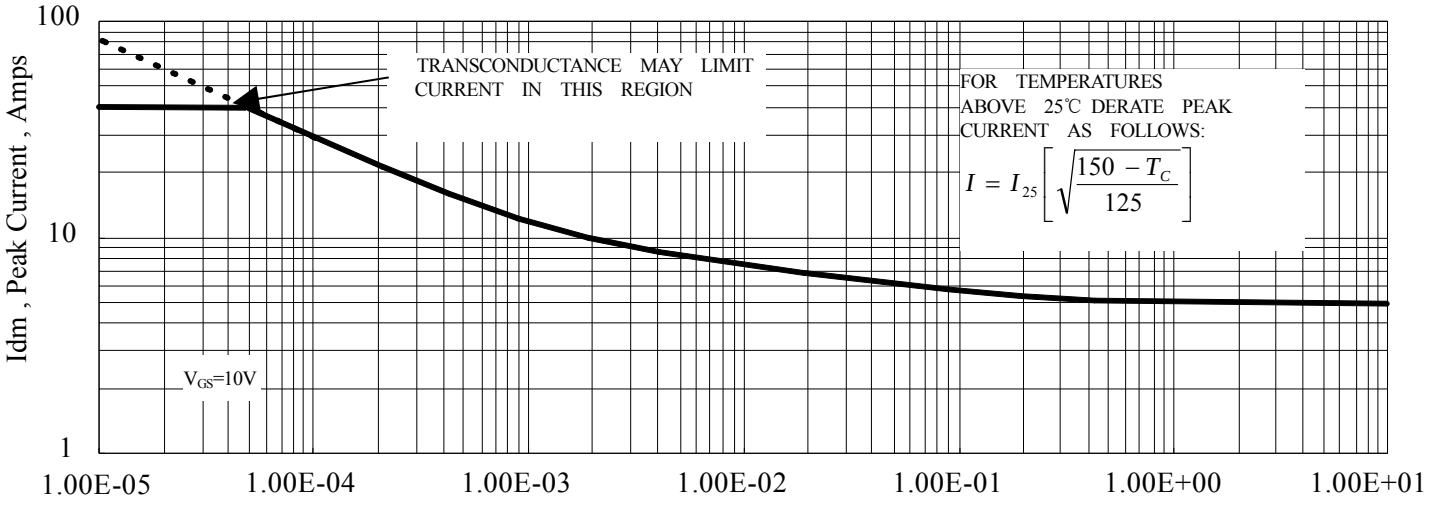


Figure 6 Maximun Peak Current Capability

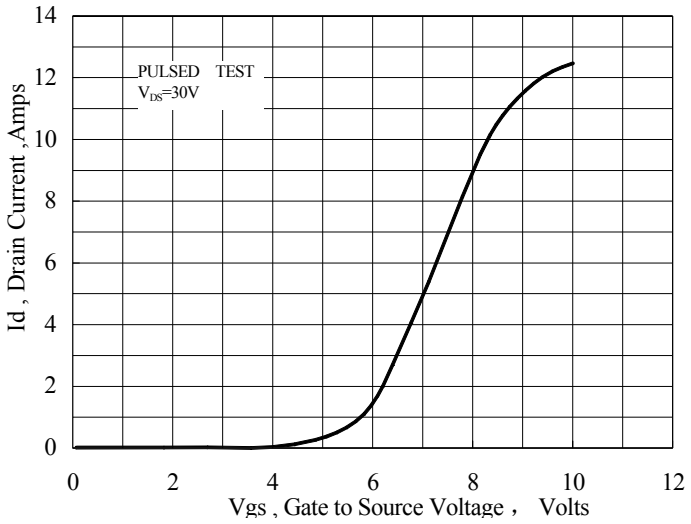


Figure 7 Typical Transfer Characteristics

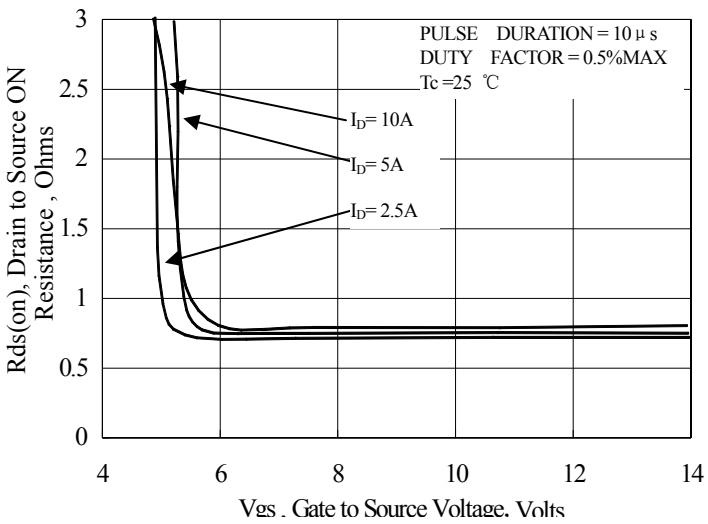


Figure 8 Typical Drain to Source ON Resistance vs Gate Voltage and Drain Current

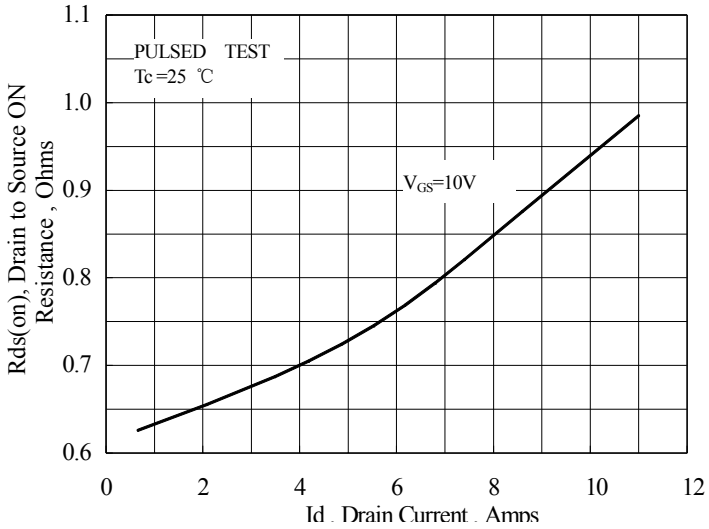


Figure 9 Typical Drain to Source ON Resistance vs Drain Current

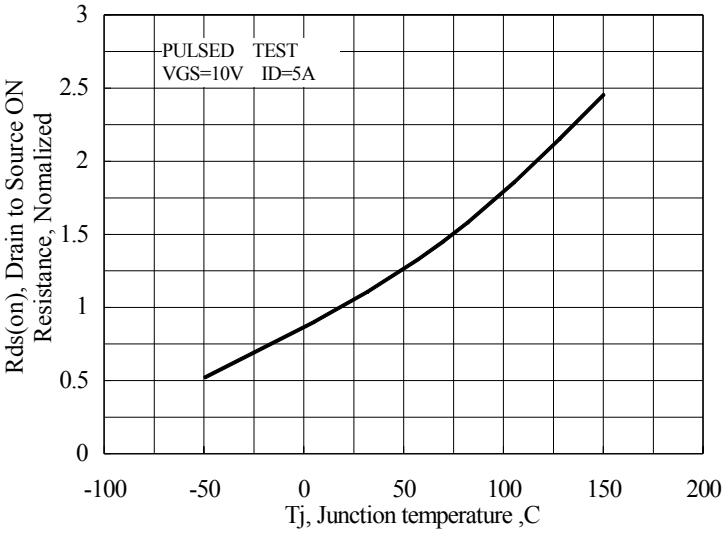


Figure 10 Typical Drian to Source on Resistance vs Junction Temperature

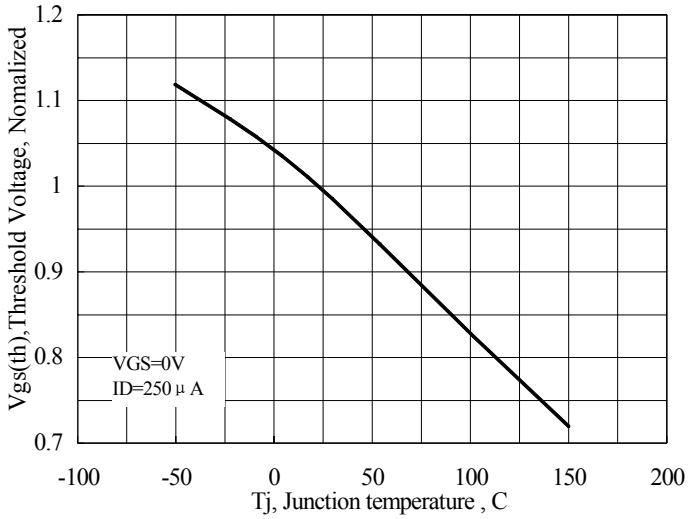


Figure 11 Typical Theshold Voltage vs Junction Temperature

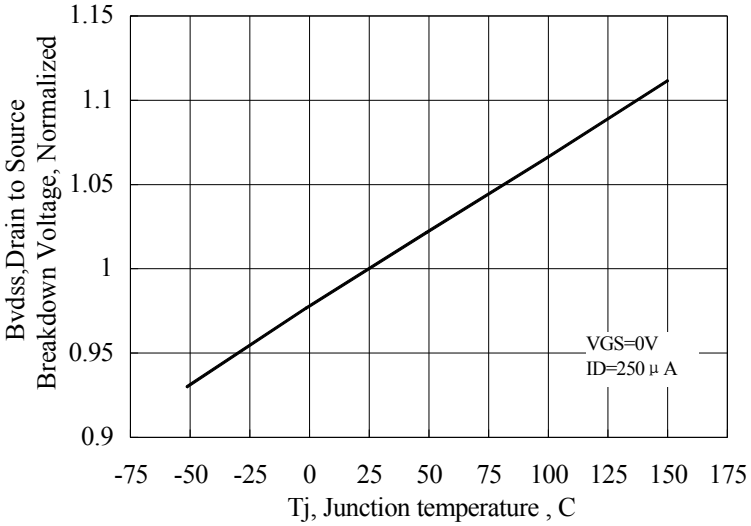


Figure 12 Typical Breakdown Voltage vs Junction Temperature

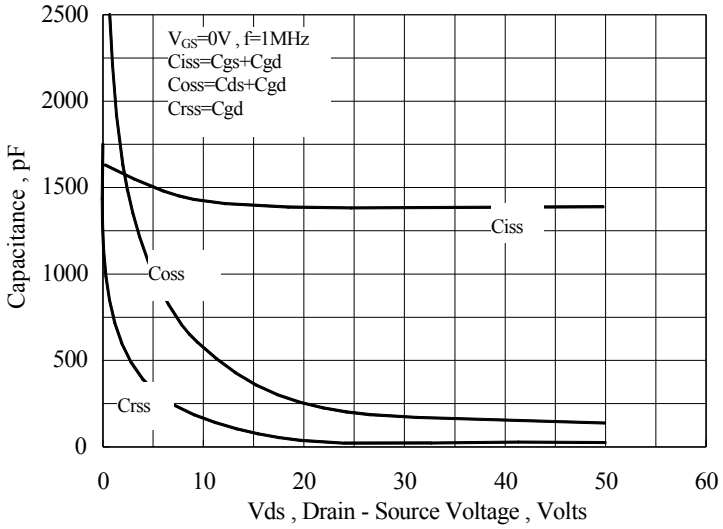


Figure 13 Typical Capacitance vs Drain to Source Voltage

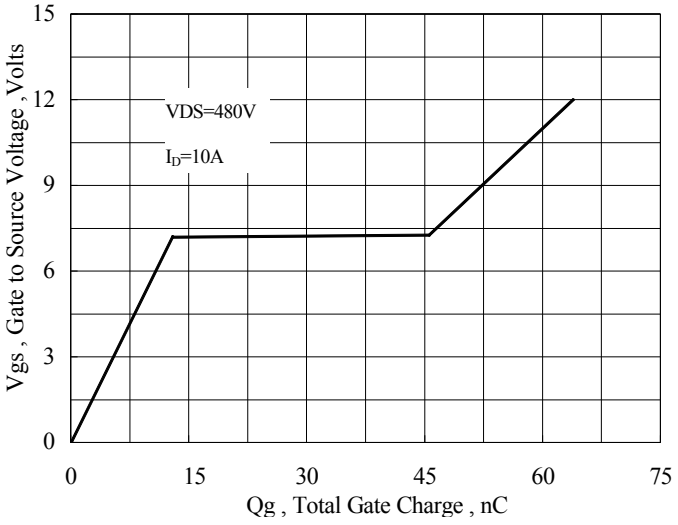


Figure 14 Typical Gate Charge vs Gate to Source Voltage

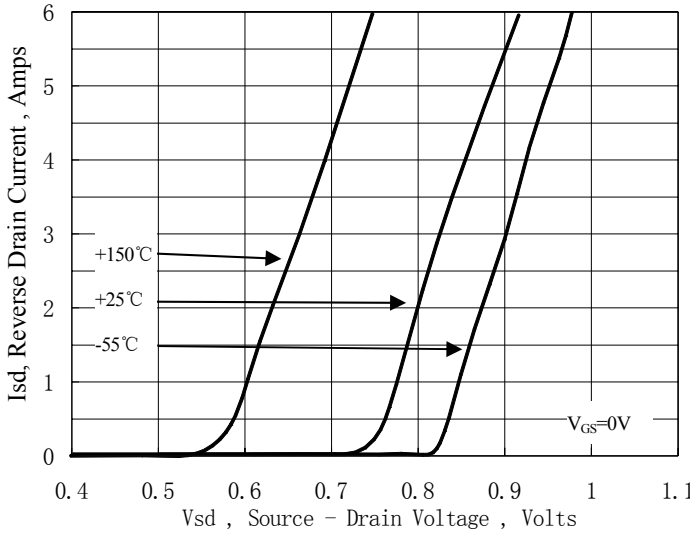


Figure 15 Typical Body Diode Transfer Characteristics

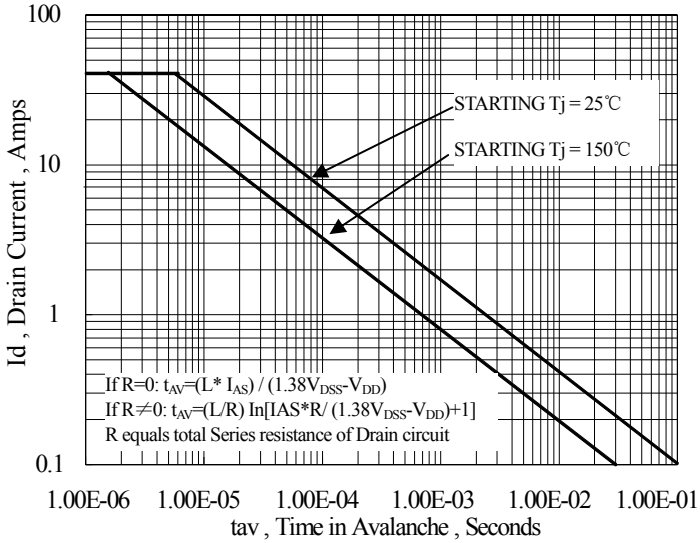
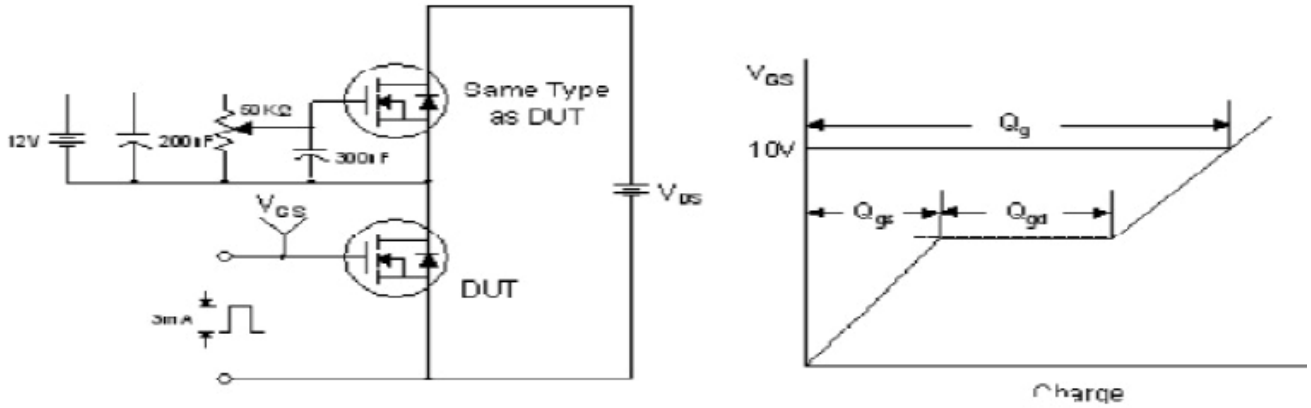
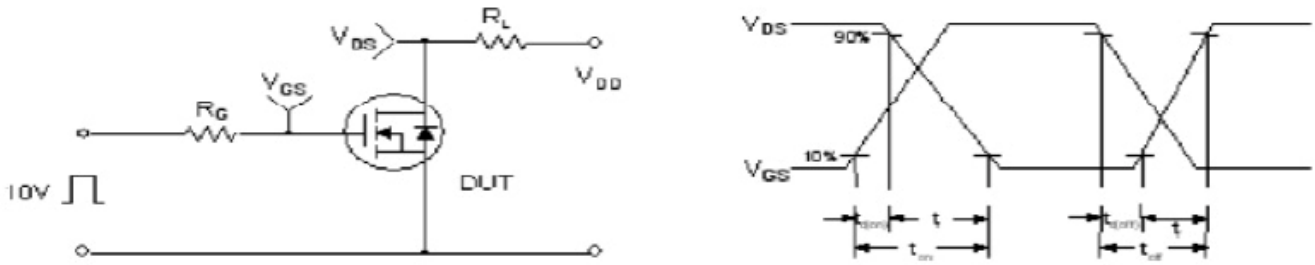


Figure 16 Unclamped Inductive Switching Capability

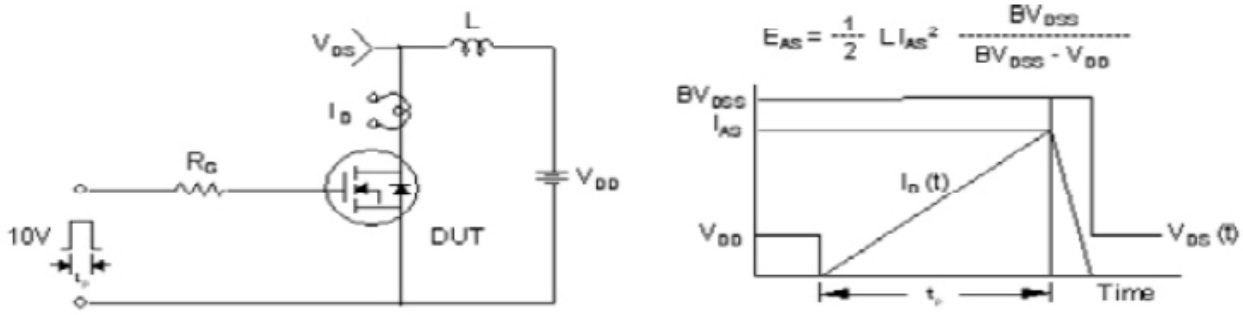
TestCircuitandWaveform



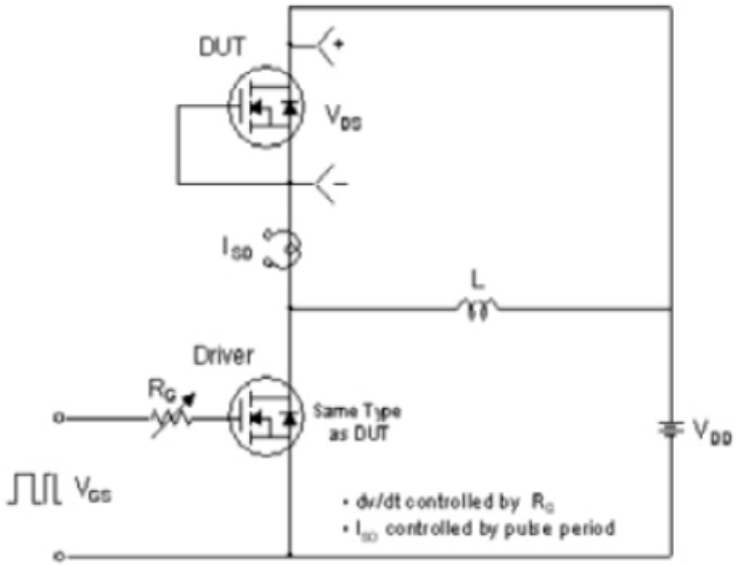
Gate Charge Test Circuit and Waveform

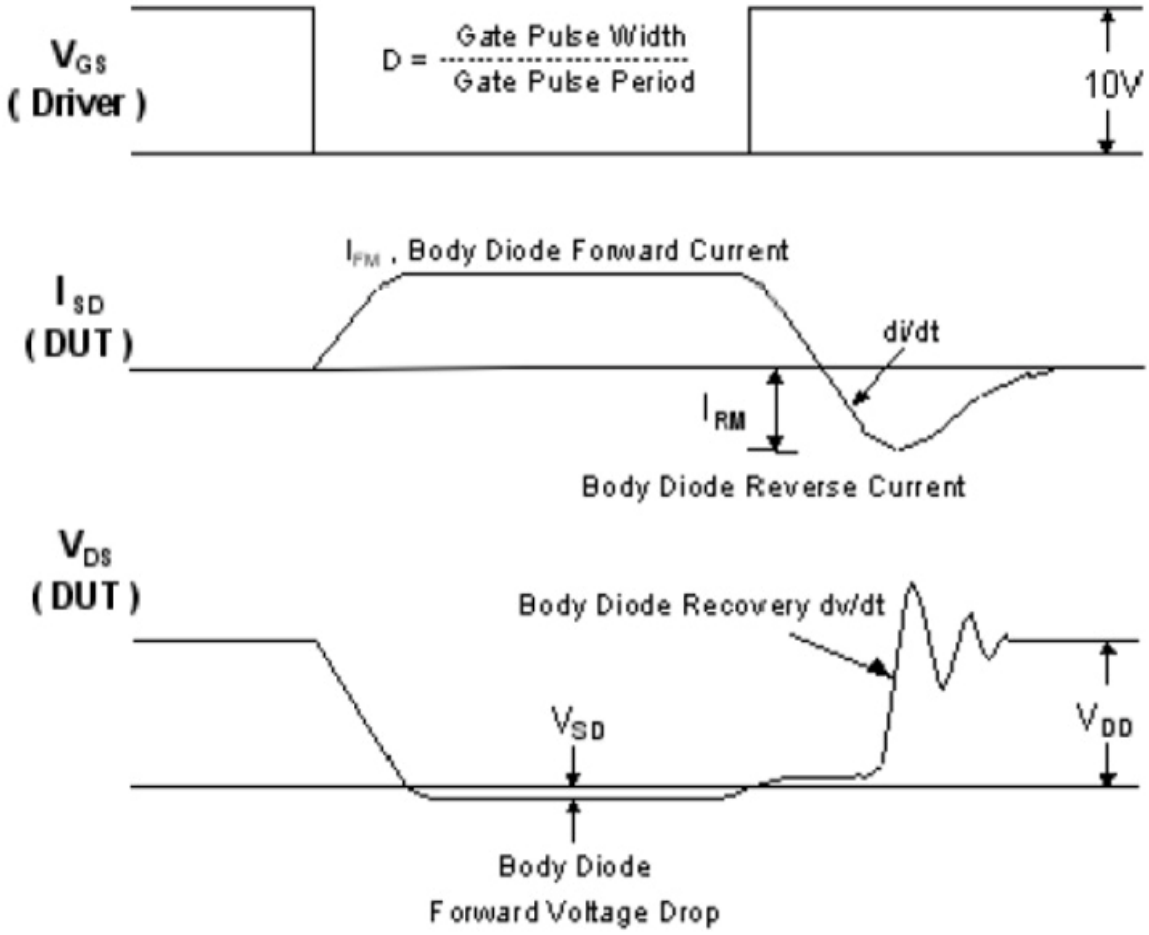


Resistive Switching Test Circuit and Waveform



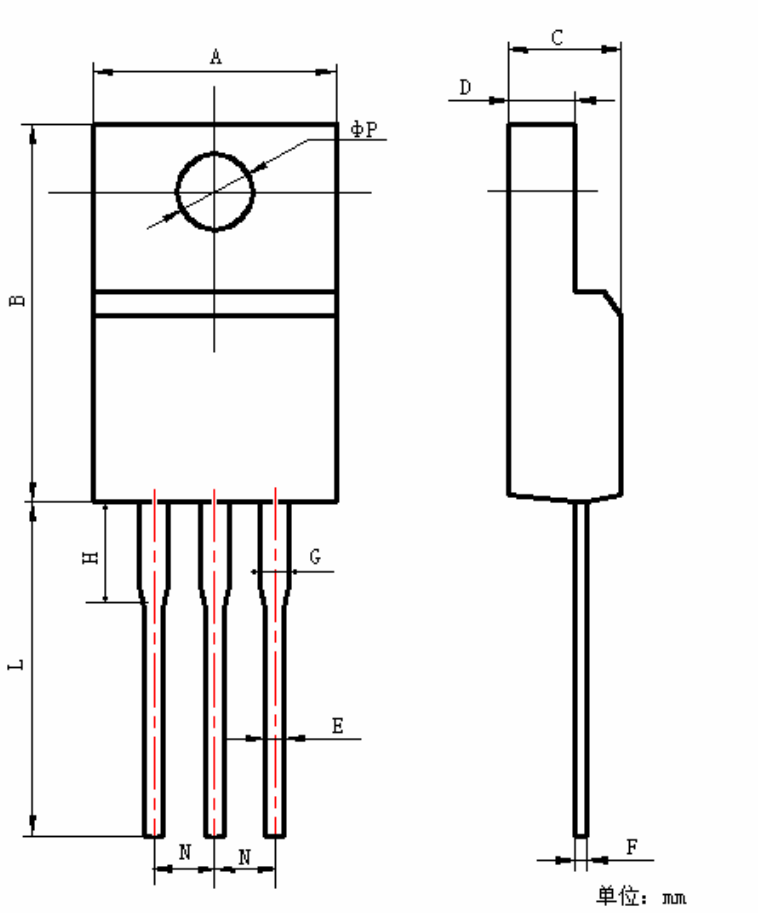
Unclamped Inductive Switching Test Circuit and Waveform





Diode Reverse Recovery Test Circuit and Waveform

Package Information：



项　目	规范(mm)	
	MIN	MAX
A	9.70	10.30
B	15.50	16.10
C	4.40	4.80
D	2.50	2.90
E	0.70	0.90
F	0.40	0.60
G	1.12	1.42
H	3.40	3.80
L	12.6	13.6
N	2.34	2.74
ΦP	3.00	3.30

TO-220F Package

The name and content of poisonous and harmful material in products

Part's Name	Hazardous Substance					
	Pb	Hg	Cd	Cr(VI)	PBB	PBDE
Limit	≤0.1%	≤0.1%	≤0.01%	≤0.1%	≤0.1%	≤0.1%
Lead Frame	○	○	○	○	○	○
Molding Compound	○	○	○	○	○	○
Chip	○	○	○	○	○	○
Wire Bonding	○	○	○	○	○	○
Solder	×	○	○	○	○	○
Note	○：means the hazardous material is under the criterion of SJ/T11363-2006. ×：means the hazardous material exceeds the criterion of SJ/T11363-2006. The plumbum element of solder exist in products presently, but within the allowed range of Eurogroup's RoHS.					

Warnings

1. Exceeding the maximun ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. It is suggested to be used under 80 percent of the maximun ratings of the device.
2. When installing the heatsink, please pay attention to the torsional moment and the smoothness of the heatsink.
3. VDMOSFETs is the device which is sensitive to the static electricity, it is necessory to protect the device from being damaged by the static electricity when using it.
4. This publication is made by Huajing Microelectronics and subject to regular change without notice.

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